A LOW NOISE GaAs MMIC SATELLITE DOWNCONVERTER FOR THE 6 to 4 GHz BAND

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ABSTRACT

An all GaAs MMIC wideband 6 to 4 GHz downconverter technology demonstrator has been designed, developed, fabricated and tested. The module achieves an overall conversion gain of 67 dB with a 3.2 dB noise figure. The MMIC chip set developed includes an LNA, an active splitter, phase shifters, a mixer, broadband power combiners and an IF amplifier. The assembly represents a significant size and weight reduction compared to conventional hybrid units.

INTRODUCTION

In order to accommodate the growing volume of communications traffic, future satellites will make increasing use of the allocated 6-4 GHz frequency bands. As a result, these satellites will carry a large number of receivers each assigned to geographically or polarisation isolated feeds. For this to be realised a new generation of miniature microwave receivers will be required. The emergence of GaAs MMIC technology makes possible the development of receivers of small size and weight, low power consumption and with radiation-hard characteristics.

This paper describes the design, MMIC implementation and packaging of a wideband 6-4 GHz technology demonstrator downconverter which incorporates a total of eighteen GaAs MMICs. Test results for the individual MMICs as well as for the complete downconverter are given and also a reliability analysis is presented.

SYSTEM DESIGN

The primary requirements for a satellite transponder front end are to:

(i) receive, amplify and frequency translate all signals in its operating band with minimum possible distortion;

(ii) to be highly reliable; and

(iii) to have the minimum achievable size, weight and DC power consumption.

A schematic of the downconverter implementation is shown in Fig. 1. The RF input, covering 5.8 to 7.1 GHz, is fed to the LNA module which comprises a Lange coupler feeding a pair of MMIC LNAs to give a low input VSWR and quadrature outputs. A passive ± 45° phase shifter MMIC cascaded with the LNA outputs then increases the output phase difference to 180° to allow balanced mixing in the mixer module.

An external 2.45 GHz local oscillator is buffered by a splitter MMIC in the LO buffer module to derive LO drive signals of suitable power and phase for the mixer.

The mixer module comprises five MMICs; a signal routing chip, two passive RF/LO combiners, a dual mixer chip and an IF amplifier chip.

The derived IF output, over the 3.4 to 4.6 GHz difference frequency band, is then filtered to remove out of band harmonics before final amplification in the post amplifier module, which comprises a cascade of six single stage MMIC amplifiers.

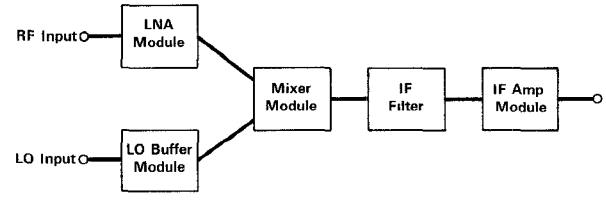

Fig. 1. Downconverter schematic

MMIC DESIGN AND PERFORMANCE

(i) LNA

The LNA is a four stage reactively matched design using 600 x 0.5μm FETs running at 15% I_{DSS} in the first two stages and 300 x 0.5μm FETs running at 50% I_{DSS} in the second two stages. Interstage matching is achieved with microstrip lines and MIM overlay capacitors with gate vias supplied through mesa isolation resistors. Drain bias is supplied through the matching network shunt lines.

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In order to enhance the yield the MMIC was laid out as two cascaded two stage chips, as shown in Fig. 2. The measured gain and noise figure of the LNA is typically 30 dB and 2 dB respectively as shown in Fig. 3. Chip size is 1.6 x 3.3 mm.

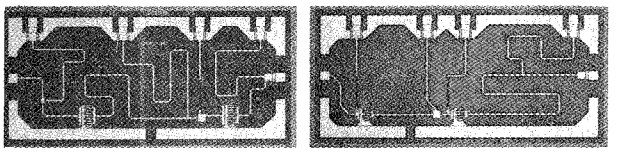

Fig. 2. Low Noise Amplifier MMIC

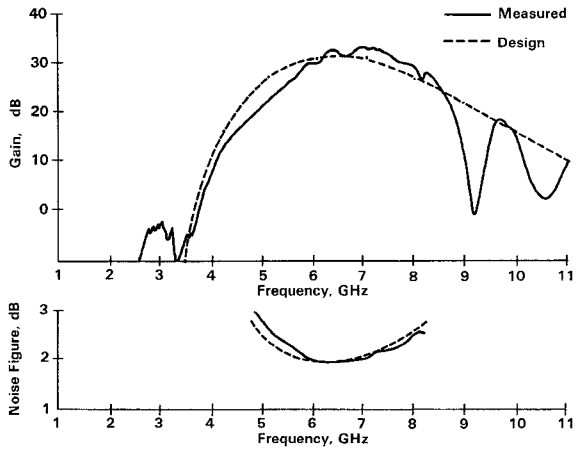

Fig. 3. LNA Gain and Noise Figure

(ii) Phase Shifters

Both the 90° (RF) and 180° (LO) phase shifter were realised as complementary high pass/low pas filters using both MIM and interdigital capacitor and spiral inductors. Measured phase shifts were typically within 6° of the required amount with insertion losses of typically 0.5 dB for the 90° circuit and 1 dB for the 180° circuit.

(iii) Local Oscillator Splitter Amplifier

The purpose of the active splitter is to buffer the LO input and to amplify and split the LO into two equal amplitude signals of sufficient level to drive the mixer FETs. A common gate input stage is used to provide a good input match and feeds two common source output FETs. Interstage matching is achieved using spiral inductors and MIM overlay capacitors. The measured gain to each output is typically 10 dB, balanced to better than 0.2 dB while the phase difference is ⩽2°. Chip size is 2.1 x 3.3 mm.

(iv) RF/LO Combiners and Mixer

Before being applied to the mixer the RF and LO signals are combined in broadband 2-section Wilkinson power combiner MMICs optimised for operation over 2-8 GHz.

The MMIC mixer is a dual common source FET design with RF/LO applied to each gate via a broadband matching network. Balancing is achieved by combining the two FET drains in a single IF output matching network. FET size is 300 x 1μm and all matching networks are realised with high impedance microstrip lines and MIM overlay capacitors. Measured conversion loss is typically 5 dB with a noise figure of 13 dB and 3rd order intercept point of +5 dBm.

(v) IF Amplifier

A resistive shunt feedback topology was chosen for this circuit function in order to provide a flat broadband gain response with good input and output matching. A photograph of the chip is shown in Fig. 4. Chip size is 1.3 x 2.8 mm. The measured performance of this chip is shown in Fig. 5 where close agreement is seen between design and measurement. Noise figure is typically 4 dB and 1 dB compressed output power is +17 dBm.

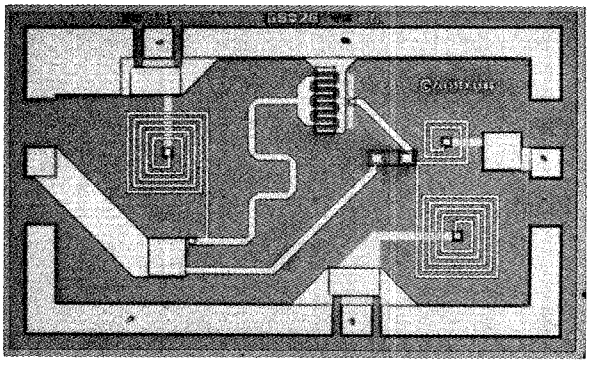

Fig. 4. IF Amplifier MMIC

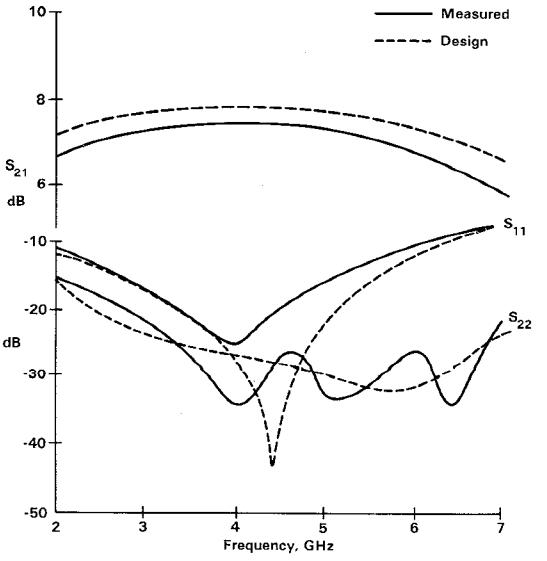

Fig. 5. IF amplifier gain and return loss

MMIC FABRICATION AND YIELD

All the circuits are fabricated on 200μm thick GaAs with active layers doped to between 1.0 and 1.8 x 10^{17} cm^{-3} depending on the circuit function. The FETs are fabricated by defining source and drain ohmic contacts by a float-off process before etching the channel to obtain the required I_{DSS}. The gates are then photolithographically printed and formed by float-off. The gate metal is also used for interconnections and overlay capacitor bottom plates. Silicon nitride is then deposited by plasma enhanced CVD for passivation and overlay capacitor dielectrics followed by a spun on layer of polyimide. The polyimide acts as a low dielectric spacing layer which supports the top level metal used for microstrip lines, spiral inductor patterns and capacitor top plates. A final silicon nitride encapsulating layer is then applied. Resistors are formed by mesa isolation of the active layer which is then etched to a suitable sheet resistance.

Included on each mask set is an array of process control monitors (PCM) which allow wafer fabrication quality to be continually assessed throughout processing. Typical yields (defined as the fraction of total die sites including PCMs and edge sites which have passed DC testing and visual screening after dicing) are 20-50% depending on circuit complexity.

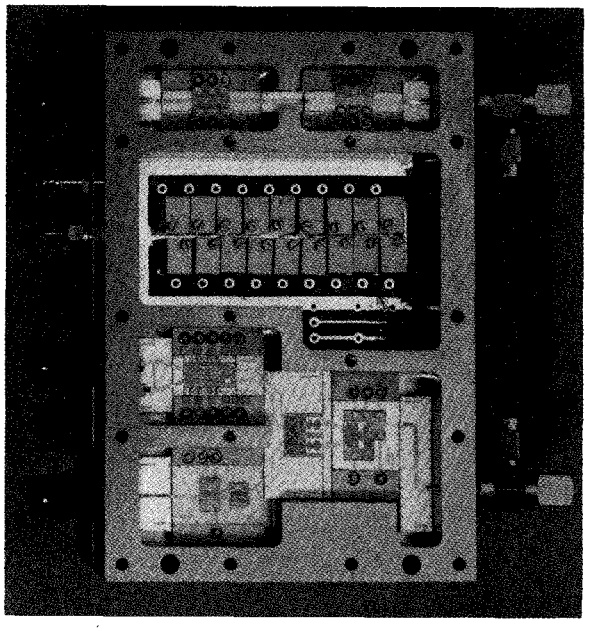

Fig. 6. Plan View of Assembled Receiver

DOWNCONVERTER CONSTRUCTION AND PERFORMANCE

A plan view photograph of a fully assembled receiver is shown in Fig. 6. The package is constructed from milled aluminium gold plated section; the top section housing the RF components and the bottom section housing a DC-DC converter. The unit measures 101 x 40 x 96 mm and weights 620 grams representing a significant reduction over comparable hybrid designs (ref. 1). The MMICs are mounted in groups on tungsten copper carriers which are linked to the DC supply via feedthroughs. The LNAs and mixer are situated in the lower half, the IF output being fed to an externally mounted bandpass filter before final amplification in the post amplifier situated in the upper half. The measured gain, noise figure and linearity are shown in Figures 7 to 9. It is believed that this is the best gain/noise figure combination reported for a MMIC subsystem of this complexity.

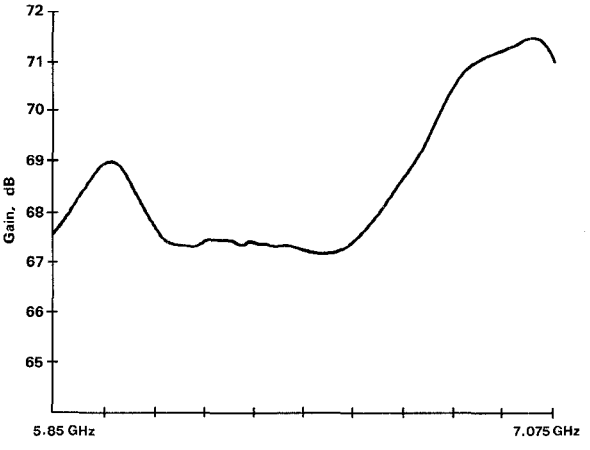

Fig. 7. Receiver Gain

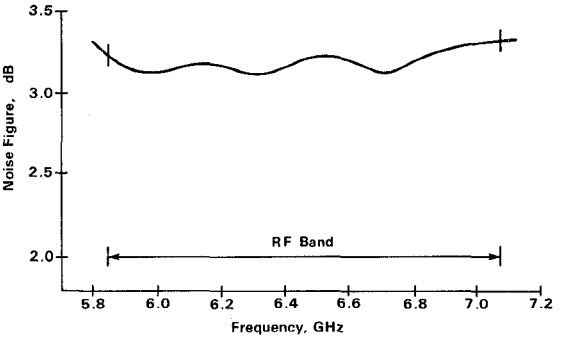

Fig. 8. Receiver Noise Figure

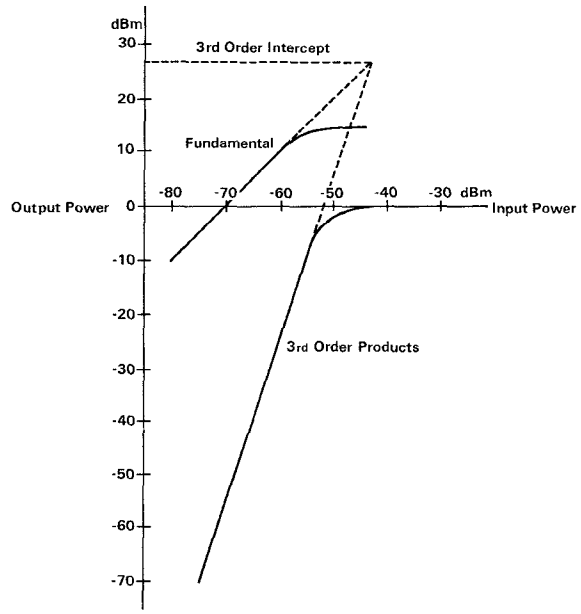

Fig. 9. Receiver Linearity

A reliability analysis was carried out on the downconverter which predicted a five year value of 79%. Due to the lack of failure rate data for GaAs MMICs these components were represented by a collection of discrete elements in the form of a hybrid microcircuit with the interconnections neglected. By reducing the electrical stres some components and increasing the level of i gration it is expected that the reliability v be substantially improved.

Some thermal vacuum tests were carried out or downconverter in which the unit was sealed vacuum chamber maintained at approx. 10^{-2} while the temperature was cycled from -40°C to +75°C. No significant performance changes were observed as a result of this test.

CONCLUSIONS

An all GaAs MMIC 6/4 GHz downconverter subsystem has been described which has achieved excellent gain and noise figure performance. The use of GaAs MMICs for all circuit functions has allowed a significant reduction in the size and weight of the unit as well as reducing the component count when compared with hybrid designs.

ACKNOWLEDGEMENTS

The authors wish to acknowledge the work of their colleagues at Plessey Research Caswell on this project.

This paper is based on work performed under the sponsorship and technical direction of the International Telecommunications Satellite Organisation (INTELSAT). Any views expressed are not necessarily those of INTELSAT.

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